

Compact Model for Low Effective Mass Channel Common Double-Gate MOSFET

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Abstract—In the spirit of quantum drift-diffusion formalism, we propose a core compact model for low-effective mass channel common double-gate MOSFET. In contrast to the existing models, carriers in each subband are treated to be in locally thermal equilibrium within that subband, but not with the carriers in a different subband. We observe quasi-linear relationship between energy eigenvalue, quasi-Fermi level, and carrier density in each subband and exploit it to obtain closed-form expressions for drain current and terminal charges. Proposed model, which is free from any unphysical model parameter or interpolating function, captures the essential device physics (strong transverse confinement, wave function penetration, multisubband occupancy, bias-dependent diffusivity, and Fermi–Dirac distribution of the carriers) while preserving the mathematical simplicity of industry standard Silicon MOSFET models. Drain current, conductance, and capacitances calculated from the proposed model are found to be in good agreement with numerical device simulation for a wide range of channel thickness, effective mass, oxide thickness asymmetry, and bias voltages.

Index Terms—III–V, compact modeling, double-gate MOSFET, drain current, quantum drift diffusion.

I. INTRODUCTION

LOW effective mass materials (III–V) are being explored extensively owing to their inherent high carrier mobility, which promises to deliver higher drive current under strict power budget [1]–[7]. Moreover, these materials could be grown over standard Silicon substrate to fabricate various electron devices [6]–[8]. However, the low effective mass leads to low density of states, and hence, there is less charge available for transport. At the same time, to preserve the electrostatic integrity, ultra-thin body multigate device architecture is required, which results in strong transverse quantum confinement. As a result, these devices demonstrate different capacitance and current characteristics compared to the conventional Si-MOSFET [9].

Development of efficient compact model is crucial for successful realization of low-effective-mass channel MOSFET-based integrated circuit. Although the Landauer formalism-based transport equation could be used to model the drain current [10], [11], due to its "position independent" nature,

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formulation of terminal charges becomes semiempirical. On the other hand, semiclassical drift-diffusion (DD) formalism has been practiced in industrial top-down compact models over the years. In this paper, we, thus, adopt the DD formalism to take the benefits arising from well-established techniques available to add different small geometry effects to the core model. However, due to the strong transverse confinement, the basic DD formalism cannot be directly applied to such MOSFETs. A suitable correction needs to be added in order to include quantum electrostatics. In case of multisubband carrier occupancy, carriers are in local equilibrium with each other in the same subband, but not with others in different subbands. Previous studies [12], [13], which are based on basic DD formalism, overlooked this fact. In other words, quantum confinement is captured only in electrostatics (i.e., in the surface potential equation) but not in transport. In addition, those models rely on unphysical model parameters or interpolating function to predict the device characteristics. Based on the quantum drift diffusion formalism, here, we propose a core model for low effective mass channel common double-gate MOSFET, which combines the solution of coupled Schrodinger–Poisson equation in the transverse direction with classical DD model in the transport direction. Individual quasi-Fermi levels for each subband are used to satisfy the above-mentioned thermal equilibrium condition. While conducting numerical simulation, we first observe quasi-linear relationships among energy eigenvalues, quasi-Fermi levels, and charge densities in each subband. We then use the recently proposed approximate solution of coupled Schrodinger–Poisson system [9] along with the aforementioned linearization scheme to obtain closed-form formulation for drain current and terminal charges without involving any unphysical model parameter or interpolating function. Such modeling techniques allow us to capture the essential device physics (strong transverse confinement, wave function penetration, multisubband occupancy, bias dependent diffusivity, and Fermi–Dirac (FD) distribution of the carriers) in a simple mathematical form, which is comparable to the core of industry standards Si MOSFET models [14], [15]. Thus, it is expected that standard techniques for adding small geometry effects practiced for Si MOSFET core model could also be applied here. The proposed model is found to be in excellent agreement with professional numerical device simulator (TCAD) [16] for wide gate and drain bias range (up to 1.5 V), channel thickness (up to 10 nm), effective mass variation (0.02–0.1), and oxide asymmetry (100%).

II. MODELING METHODOLOGY

The expression for drain-to-source current I_{DS} under quantum DD formalism along transport (y) direction in a common

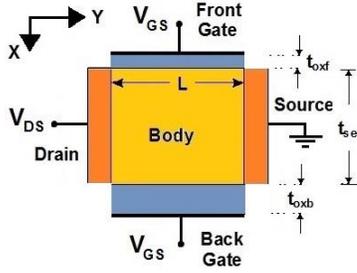


Fig. 1. Schematic of the common double-gate MOSFET with asymmetric oxide thickness.

double-gate MOSFET could be written as [17]

$$I_{DS} = \sum_{i=1}^{n_{\max}} I_{DS,i} = -W \sum_{i=1}^{n_{\max}} \left[\mu_i Q_{se,i} \frac{dE_i}{dy} - D_i \frac{dQ_{se,i}}{dy} \right]. \quad (1)$$

The schematic of the structure is given in Fig. 1. Here, the subscript i refers to subband index. $I_{DS,i}$ is the drain-to-source electron current, $Q_{se,i}$ is the charge density, n_{\max} is the maximum number of energy subbands (in this work ranges from 1 to 3), I_{DS} is the total current contribution due to all n_{\max} subbands, E_i subband energy (Eigen value), μ_i is the carrier mobility, D_i is the carrier diffusivity, and W is the channel width. $Q_{se,i}$ is calculated from solutions of coupled Schrodinger–Poisson equation in transverse direction taking into account the wavefunction penetration into gate oxide along with FD statistics and asymmetry in gate oxide thickness [9], and expressed as follows:

$$Q_{se,i} = U_t C_{q,i} \ln \left(1 + e^{\left[\frac{E_{F,i} - E_i}{kT} \right]} \right). \quad (2)$$

Here, $U_t = kT/q$, $E_{F,i}$ and $C_{q,i}$ are the quasi-Fermi level and the associated capacitance term for i -th subband, respectively [9]. E_i can be calculated from the recently proposed approximate solution of the coupled Schrodinger-Poisson equation [9] as given by the following implicit equation:

$$(C_{oxf}^e + C_{oxb}^e)(V_G - \phi_m) = U_t \sum_{i=1}^{n_{\max}} Q_{se,i} \quad (3)$$

with

$$E_i = E_i^{(0)} - q\phi_m - M_i'(V_G - \phi_m) - M_i''(V_G - \phi_m)^2 + \frac{E_{g,se}}{2}. \quad (4)$$

Here, $E_i^{(0)}$ is the subband energy under flat-band condition, $E_{g,se}$ is the band gap of the channel material, M_i' and M_i'' are coefficients of the first- and second-order energy perturbation terms, respectively [9], V_G is the effective gate voltage, and ϕ_m is the electrostatic potential at zero electric field point inside the channel. It is to be noted that while calculating charge density in [9], the second-order perturbation was used for only 3rd subband to keep the computational budget low. In this paper, we include the second order perturbation in all the subbands, to accurately capture the effect of lateral and transverse electric fields in quantum DD. Hence, unlike [9], M_i'' is nonzero for every subband. Using (2) and (4), ϕ_m is

calculated from the equation of charge density (3) derived in [9].

In addition, it should be noted that the above-mentioned Poisson–Schrodinger solution has been developed based on "particle in a box" formalism, which is simple and intuitive, easily transferable to any low effective mass channel material, and successfully used in ultrathin body Si-MOSFET modeling [18]. More rigorous first principle-based band structure calculation method (density functional theory, tight binding, etc.) is material (crystal structure) specific, computationally expensive, and thus not fit for compact modeling purpose. It is worth noting that the surface potential equation (3) has been validated [9] for valley degeneracy factor $g_v = 1$, since it is applicable to most of the III–V materials being explored for MOSFET channels. It may be extended to higher values of g_v by multiplying the $C_{q,i}$ term with g_v (which is basically multiplying the right-hand side of [9, eq. (3)] by g_v) and appropriately modifying the compensation factors (C-5) and (C-6) of [9]. It should further be noted that subband degeneracy is one in our case due to 1-D confinement.

It is worth mentioning that due to 2-D electron gas within the ultrathin channel and FD statistics, Einstein's relation D_i/μ_i takes a bias-dependent form [19], which, if used directly, would complicate the model. To avoid complexity, we use the fact that at zero drain-to-source bias, the drain current has to be zero, and thus, $D_i = \mu_i Q_{se,i} (dE_i/dQ_{se,i})$. Now setting $\mu = \mu_i \forall i$, following similar steps as in [13], we arrive at:

$$I_{DS} = \sum_{i=1}^{n_{\max}} I_{DS,i} = -\mu W \sum_{i=1}^{n_{\max}} Q_{se,i} \frac{dE_{F,i}}{dy}. \quad (5)$$

Under dc bias condition, as the total current I_{DS} is constant at any y , integrating both sides of (5) with respect to y under limits $y \in \{0, L\}$, we get

$$I_{DS} = -\mu \left(\frac{W}{L} \right) \sum_{i=1}^{n_{\max}} \int_{E_{FS}}^{E_{FD}} Q_{se,i} dE_{F,i} \quad (6)$$

where E_{FS} and E_{FD} are $E_{F,i}$ at source and drain, respectively, and L is the channel length. When carriers are settled in distantly separated multiple energy subbands, they are in a local thermal equilibrium within their own subbands which results in separate quasi-Fermi level for each subband. A major merit of this paper lies in taking into account the segregation of subband Fermi levels, which was ignored in the previous work [13]. Although physically justifiable, incorporation of the three separate quasi-Fermi levels poses a new challenge in the core model development. Evidently from the expression of surface potential equation (3), values for $E_{F,i}$ are different for each subbands except at source and drain end where they thermalize to E_{FS} and E_{FD} , respectively. Without any prior knowledge of all $E_{F,i}$, it is therefore not possible to solve (3) at any position within the source and drain. Such problem does not arise in case of Si MOSFET models as they deal with single quasi-Fermi level, and quantum confinement effect is added as a correction to the core model through "band-gap broadening" formalism [15].

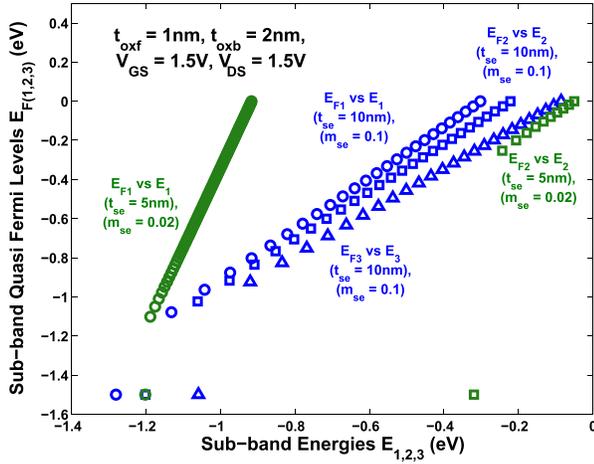


Fig. 2. Subband quasi-Fermi level variation with subband energy along the channel for given bias condition. Right and left ends of each characteristic represent their values at source and drain ends, respectively.

In this paper, we propose a unique way of calculating (6) by appropriately linearizing the integrand. A pursuit of direct solution of (6) generates complicated expression involving interpolating functions [13]. We discuss the linearization scheme in next section, and show in detail in the subsequent sections how this leads to a simple yet accurate compact model fit for implementing in a circuit simulator.

III. CHARGE LINEARIZATION TECHNIQUE

Charge linearization techniques [20] have played a major role in developing the ‘compact’ form of drain current expression in different industry standard Si MOSFET models [14], [15]. This helps to express drain current in a quadratic function of surface-potential/charge-density, which could be further used to obtain an invertible relation between lateral position in the channel and surface-potential/charge-density. Such a relationship is very useful in developing quasi-static and nonquasi-static expressions for terminal charges [14], [21], [22] using Ward–Dutton partition scheme [23]. In this paper, we first conducted numerical device simulation to explore the possibility of suitable charge linearization scheme, which could be exploited to obtain a compact form of drain current and terminal charges.

The numerical device simulation is conducted using ATLAS numerical device simulator, a part of Silvaco TCAD suite [16]. The quantum transport model is implemented using mode-space approach (in DDMS module) [24], where the solution is decoupled into the Schrodinger equation in transverse direction and 1-D classical DD in each subband. Thus, the formalism captures quantum effects in transverse direction, and yet inherits all familiar models for field-dependent mobility, which could be attached to basic DD equations.

From these simulations, we observe quasi-linear relationship among subband quasi-Fermi levels, subband charge density ($N_i = Q_{se,i}/q$), and subband energies as shown in Figs. 2 and 3. The parametric range used involves device with lowest ($t_{se} = 10$ nm, $m_{se} = 0.1$) and highest confinement

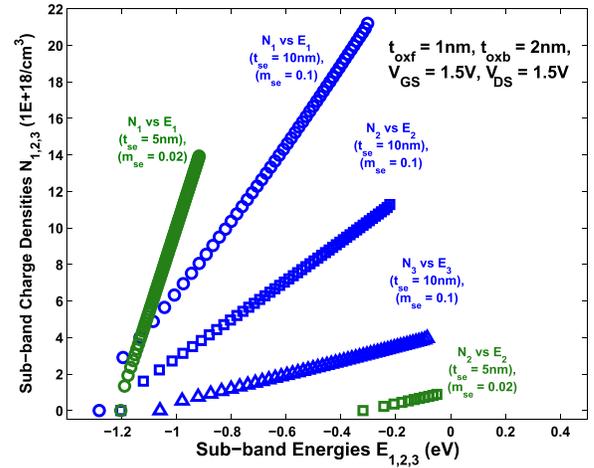


Fig. 3. Subband charge density variation with subband energy along the channel for given bias condition. Right and left ends of each characteristic represent their values at source and drain ends, respectively.

($t_{se} = 5$ nm, $m_{se} = 0.02$) under extreme gate-to-source ($V_{GS} = 1.5$ V) and drain-to-source ($V_{DS} = 1.5$ V) bias conditions, to ensure the infallibility of charge linearization scheme within that range. Common low effective mass channel materials like InAs, $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$, GaAs, InP, and so on fall under this range having effective masses approximately 0.024, 0.04, 0.068, and 0.08, respectively. The reason behind such a linear relationship may be explained in the following manner: as the electrostatic potential increases along the channel, the subband energy levels drop, and hence, the thermodynamic work required to add one electron to each subband, which is the electrochemical potential or approximately the Fermi energy [25], also drops in equal proportion. We exploit this behavior by expressing $Q_{se,i}$ as a linear function of E_i

$$Q_{se,i} = a_{0,i} + a_{1,i}E_i. \quad (7)$$

Here, $a_{0,i}$ and $a_{1,i}$ are linearization constants and are evaluated by applying boundary condition on (7) at source ($E_i = E_{i(S)}$, $Q_{se,i} = Q_{se,i(S)}$) and at drain ($E_i = E_{i(D)}$, $Q_{se,i} = Q_{se,i(D)}$). $E_{i(S)}$, $Q_{se,i(S)}$, and $E_{i(D)}$, $Q_{se,i(D)}$ can be obtained from (2)–(4) by applying $E_{F,i} = 0$ and $E_{F,i} = -V_{DS}$, respectively. $a_{0,i}$ and $a_{1,i}$ are given as follows:

$$a_{0,i} = \frac{Q_{se,i(S)}E_{i(D)} - Q_{se,i(D)}E_{i(S)}}{E_{i(D)} - E_{i(S)}}$$

$$a_{1,i} = \frac{Q_{se,i(D)} - Q_{se,i(S)}}{E_{i(D)} - E_{i(S)}}.$$

It trivially follows from (7) that $dQ_{se,i}/dE_i = a_{1,i}$. In Section IV, we develop the drain current model utilizing (7) and quasi-linear behavior of $E_{F,i}$ versus E_i .

IV. DRAIN CURRENT AND TERMINAL CHARGE MODELING

We start developing our model by changing the variable in (6) from $dE_{F,i}$ to dE_i

$$I_{DS} = -\mu \left(\frac{W}{L} \right) \sum_{i=1}^{n_{\max}} \int_{E_{i(S)}}^{E_{i(D)}} Q_{se,i} \frac{dE_{F,i}}{dE_i} dE_i. \quad (8)$$

From Fig. 2, it is clear that $E_{F,i}$ and E_i are linearly dependent everywhere in the channel except near vicinity of drain region, even under very high bias ($V_{GS} = 1.5$ V, $V_{DS} = 1.5$ V). We may safely ignore this sudden non-linearity in $E_{F,i}$ versus E_i characteristic, as charge contribution of that region is very less when V_{DS} is very high and the drain current approaches saturation. Thus, we may reasonably put $(dE_{F,i}/dE_i) = (dE_{F,i}/dE_i)_{(S)} = K_{P,i}$, where $K_{P,i} = (dE_{F,i}/dE_i)$ evaluated at source. The expression of the prefactor $K_{P,i}$ is derived in (A-3) of the Appendix. Hence, I_{DS} is given by

$$I_{DS} = -\mu \left(\frac{W}{L} \right) \sum_{i=1}^{n_{\max}} K_{P,i} \int_{E_i(S)}^{E_i(D)} Q_{se,i} dE_i. \quad (9)$$

Using (7) and changing variable from E_i to $Q_{se,i}$ in (9), we get the final expression for I_{DS} as

$$I_{DS} = -\mu \left(\frac{W}{L} \right) \sum_{i=1}^{n_{\max}} K_{Pr,i} [Q_{se,i(D)}^2 - Q_{se,i(S)}^2]. \quad (10)$$

Here, $K_{Pr,i} = (K_{P,i}/2a_{1,i})$. Equation (10) represents a purely physical compact drain current model for quantum well common double-gate MOSFETs. Similar to state-of-the-art Si MOSFET models [15], it is a single piece equation which is valid for different regimes of transistor operation. For a constant V_{GS} , as V_{DS} increases, $Q_{se,i(D)}$ becomes negligible with respect to $Q_{se,i(S)}$, as is evident from Fig. 3. As a result, at high V_{DS} , the drain current depends only on $Q_{se,i(S)}$ and $K_{P,i}$, which are constants due to constant V_{GS} . This is how the proposed model captures the drain current saturation.

Derivation of the closed form analytical expression for terminal charges requires working out the y versus $Q_{se,i}$ relationship, which is readily obtained from (5) and (10), and is given by

$$y = \frac{Q_{se,i}^2 - Q_{se,i(S)}^2}{Q_{se,i(D)}^2 - Q_{se,i(S)}^2} L. \quad (11)$$

So, the gate terminal charge $Q_G = W \sum_{i=1}^{n_{\max}} \int_0^L Q_{se,i} dy$ is obtained from (11) given by

$$Q_G = \left(\frac{2WL}{3} \right) \sum_{i=1}^{n_{\max}} \frac{Q_{se,i(D)}^3 + Q_{se,i(S)}^3 + Q_{se,i(D)} Q_{se,i(S)}}{Q_{se,i(D)}^2 + Q_{se,i(S)}^2}. \quad (12)$$

Using Ward–Dutton charge partition formula [23], we calculate total drain terminal charge $Q_D = -W \sum_{i=1}^{n_{\max}} \int_0^L (y/L) Q_{se,i} dy$ using (11).

From (12) and (13), the source terminal charge could be obtained using the charge neutrality condition as $Q_S = -Q_G - Q_D$. Thus, completely physical models of terminal charges are developed unlike previous works [13], as shown at the bottom of the next page, where the inversion charge profile is interpolated using a quadratic polynomial making Q_D a function of Q_G . The proposed model bears the same level of compactness and simplicity as the industry standard models of Si-MOSFET [14], [15].

This paper is based on parabolic band approximation. In case of strong nonparabolicity, the effective mass will become carrier energy dependent. As here we are using

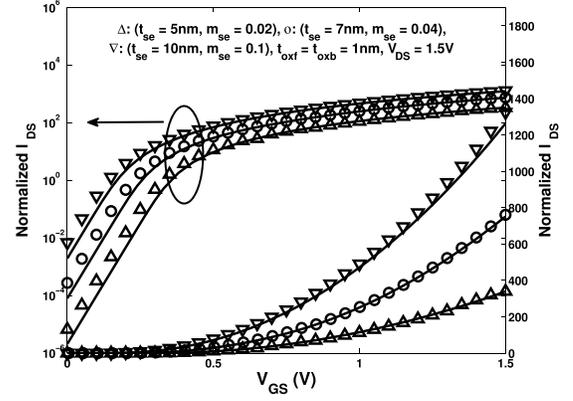


Fig. 4. Variation of normalized drain current of symmetric device with effective gate-to-source voltage (line: model and symbol: TCAD).

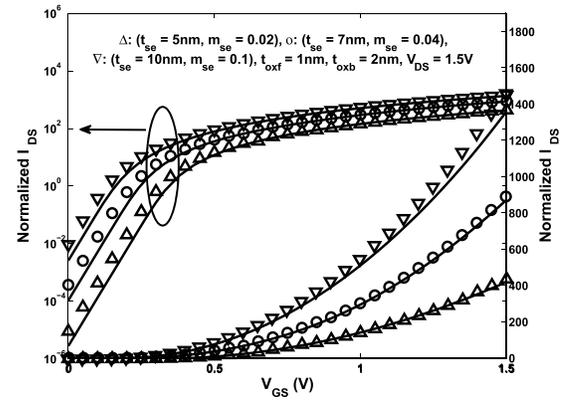


Fig. 5. Variation of normalized drain current of asymmetric device with effective gate-to-source voltage (line: model and symbol: TCAD).

constant mobility model, it is not possible to inculcate nonparabolicity effect in the core model. However, when the small geometry effects are added to the core in an industry-standard top-down formalism, the electric field-dependent mobility model can be parameterized to capture this effect.

V. RESULTS AND DISCUSSION

The proposed models of drain current (10) and total charge at gate (12) have been validated against the numerical device simulator [16]. Under simulation environment, to solve the coupled Schrodinger–Poisson equations inside oxide and semiconductor, we used SCHRO and OX.SCHRO commands, and to solve the DD transport under transverse quantum confinement, we used DD_MS command. The fixed material parameters used are: $V_{ox} = 3.9$ eV, $V_{se} = 0.133$ eV, $\epsilon_{se} = 13.6 \epsilon_0$ and $\epsilon_{ox} = 3.9 \epsilon_0$, ϵ_0 being the permittivity of free space, $W = 1 \mu\text{m}$, and $L = 1 \mu\text{m}$. All the effective masses are multiplied with m_0 , the free electron mass.

All the plots of drain current, capacitance, and transconductance are normalized by factors $I_0 = \mu(W/L)C_{ox,av}U_t^2$, $C_0 = WLC_{ox,av}$, and $G_{m,0} = \mu(W/L)C_{ox,av}U_t$, respectively. Here, $C_{ox,av} = (C_{oxf} + C_{oxb})/2$ is the average of the front and back oxide capacitances.

Figs. 4 and 5 show the variation of normalized drain current with respect to effective gate-to-source voltage both in linear

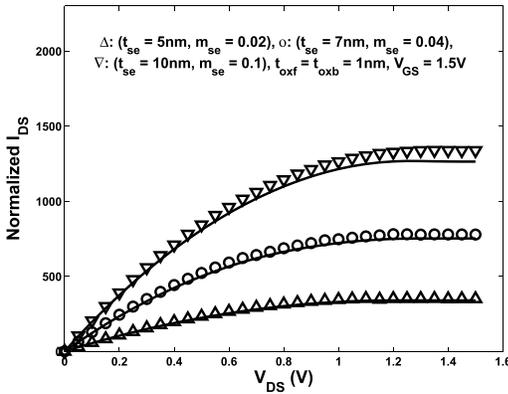


Fig. 6. Variation of normalized drain current of symmetric device with drain-to-source voltage (line: model and symbol: TCAD).

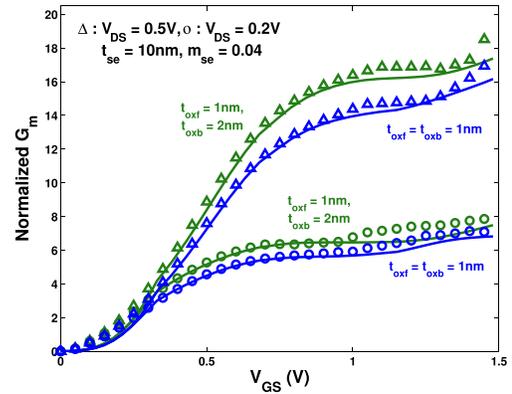


Fig. 8. Variation of normalized transconductance with effective gate-to-source voltage (line: model and symbol: TCAD).

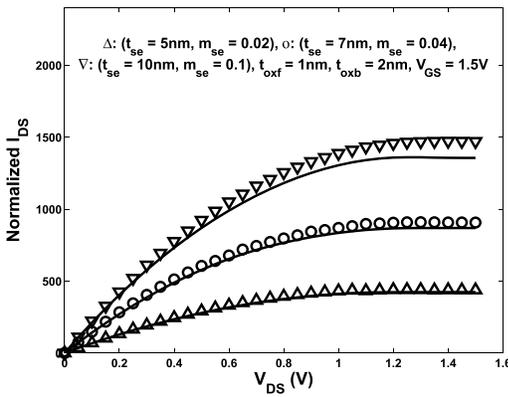


Fig. 7. Variation of normalized drain current of asymmetric device with drain-to-source voltage (line: model and symbol: TCAD).

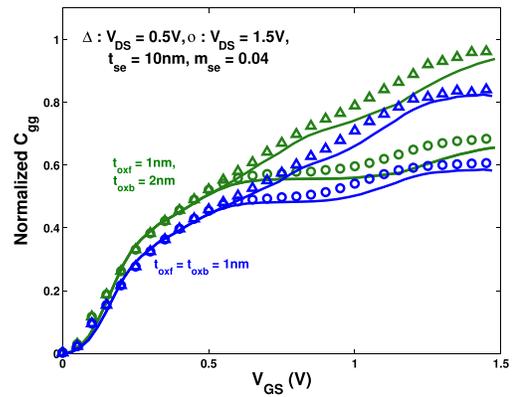


Fig. 9. Normalized gate capacitance versus effective gate voltage (line: model and symbol: TCAD).

and logarithmic scales for symmetric and asymmetric devices, respectively. As is evident, the model yields good agreement with TCAD simulation over different thickness and effective masses of channel material.

The variation of normalized drain current with respect to drain-to-source voltage for different material parameters are shown in Figs. 6 and 7 for symmetric and asymmetric devices, respectively. Fig. 8 corroborates the effectiveness of the drain current model, as simulated transconductance matches quite satisfactorily with that predicted by derivative of proposed drain current model for different biasing conditions and device parameters. Figs. 9 and 10 validate the terminal gate charge model (12). The simulated gate capacitance and gate-to-drain capacitance appear to be in good agreement with the model. Fig. 11 demonstrates the drain-to-gate capacitance model, which is the derivative of partitioned drain terminal charge (13), with respect to effective gate voltage. Validation of this model with TCAD data was not possible as it is not possible to conduct small signal analysis under quantum

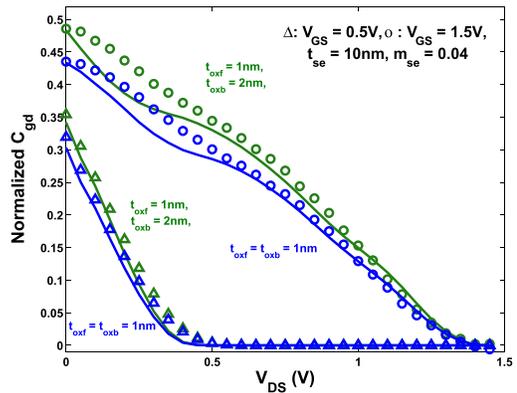


Fig. 10. Normalized gate-to-drain capacitance versus drain voltage (line: model and symbol: TCAD).

drift diffusion simulation. However, calculation of Q_G does not incur this problem, as it could be calculated from dc simulation. The agreement between model and TCAD data is

$$Q_D = - \left(\frac{2WL}{15} \right) \sum_{i=1}^{n_{\max}} \frac{3Q_{se,i(D)}^3 + 2Q_{se,i(S)}^3 + 6Q_{se,i(D)}^2 Q_{se,i(S)} + 4Q_{se,i(D)} Q_{se,i(S)}^2}{(Q_{se,i(D)} + Q_{se,i(S)})^2}$$

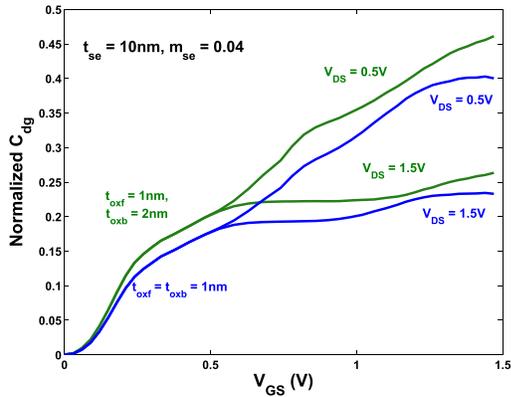


Fig. 11. Normalized drain-to-gate capacitance versus effective gate voltage.

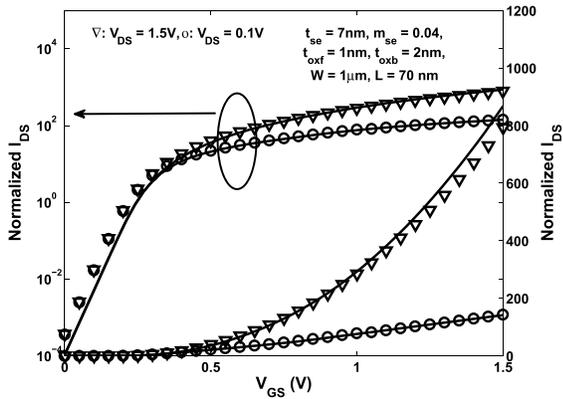


Fig. 12. Variation of normalized drain current of asymmetric shorter channel device with effective gate-to-source voltage (line: model and symbol: TCAD).

remarkable, although no unphysical model parameter or interpolating function is involved. We further show that the proposed model is also applicable for short channel devices (Fig. 12) as long as gradual channel approximation holds good.

VI. CONCLUSION

We propose a fully physical quantum DD-based core compact model for low DOS material channel common double-gate MOSFET. We employ a novel charge linearization scheme, which enabled us to obtain simple and compact expressions for drain current and terminal charges without ever using any fitting parameter or interpolating function. The models have been extensively validated over a broad range of device as well as material parameters along with bias against numerical device simulations. Proposed compact modeling technique, thus, allow us to extend the quantum DD formalism for circuit simulation, which has so far been limited to device simulation.

APPENDIX

The inversion charge in i th subband is given by (2). Differentiating both sides, we get

$$\frac{dQ_{se,i}}{dE_i} = \frac{C_{q,i}/q}{1 + e^{\left[\frac{E_i - E_{F,i}}{kT}\right]}} \left(\frac{dE_{F,i}}{dE_i} - 1 \right). \quad (\text{A-1})$$

Again using the quasi-linear behavior of $Q_{se,i}$ versus E_i , as discussed in Section III, we have $dQ_{se,i}/dE_i = a_{1,i}$. Thus, we arrive at

$$\frac{dE_{F,i}}{dE_i} = 1 + a_{1,i} \frac{q}{C_{q,i}} \left(1 + e^{\left[\frac{E_i - E_{F,i}}{kT}\right]} \right). \quad (\text{A-2})$$

Hence, $K_{P,i} = (dE_{F,i}/dE_i)_{(S)}$ is obtained by substituting $E_i = E_{i(S)}$ and $E_{F,i} = E_{FS} = 0$ in (A-2)

$$K_{P,i} = 1 + a_{1,i} \frac{q}{C_{q,i}} \left[1 + e^{\frac{E_{i(S)}}{kT}} \right]. \quad (\text{A-3})$$

REFERENCES

- [1] (2013). *International Technology Roadmap for Semiconductors*. [Online]. Available: <http://www.itrs2.net>
- [2] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, pp. 317–323, Nov. 2011, doi: 10.1038/nature10677.
- [3] Y. Sun *et al.*, "High-performance CMOS-compatible self-aligned $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFETs with GMSAT over $2200 \mu\text{S}/\mu\text{m}$ at $V_{DD} = 0.5 \text{ V}$," in *IEDM Tech. Dig.*, Dec. 2014, pp. 25.3.1–25.3.4, doi: 10.1109/IEDM.2014.7047106.
- [4] Y. Kamata, "High- k/Ge MOSFETs for future nanoelectronics," *Mater. Today*, vol. 11, nos. 1–2, pp. 30–38, 2008, doi: 10.1016/S1369-7021(07)70350-4.
- [5] S. Adachi, *Properties of Group-IV, III-V and II-VI Semiconductors*. Hoboken, NJ, USA: Wiley, 2005, doi: 10.1002/0470090340.
- [6] H. Schmid *et al.*, "Monolithic integration of multiple III-V semiconductors on Si for MOSFETs and TFETs," in *IEDM Tech. Dig.*, Dec. 2016, pp. 3.6.1–3.6.4, doi: 10.1109/IEDM.2016.7838340.
- [7] M. K. Hudait and R. Chau, "Integrating III-V on silicon for future nanoelectronics," in *Proc. IEEE Compound Semicond. Integr. Circuits Symp. (CSIC)*, Oct. 2008, pp. 1–2, doi: 10.1109/CSICS.2008.8.
- [8] M. K. Hudait *et al.*, "Heterogeneous integration of enhancement mode $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ quantum well transistor on silicon substrate using thin ($< 2 \mu\text{m}$) composite buffer architecture for high-speed and low-voltage (0.5 V) logic applications," in *IEDM Tech. Dig.*, Dec. 2007, pp. 625–628, doi: 10.1109/IEDM.2007.4419017.
- [9] A. S. Chakraborty and S. Mahapatra, "Surface potential equation for low effective mass channel common double-gate MOSFET," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1519–1527, Apr. 2017, doi: 10.1109/TEDE.2017.2661798.
- [10] M. S. Lundstrom and D. A. Antoniadis, "Compact models and the physics of nanoscale FETs," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 225–233, Feb. 2014, doi: 10.1109/TEDE.2013.2283253.
- [11] S. Oh and H.-S. P. Wong, "A physics-based compact model of III-V FETs for digital logic applications: Current-voltage and capacitance-voltage characteristics," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2917–2924, Dec. 2009, doi: 10.1109/TEDE.2009.2033411.
- [12] C. Yadav, M. Agrawal, A. Agarwal, and Y. S. Chauhan, "Compact modeling of charge, capacitance, and drain current in III-V channel double gate FETs," *IEEE Trans. Nanotechnol.*, vol. 16, no. 2, pp. 347–354, Mar. 2017, doi: 10.1109/TNANO.2017.2669092.
- [13] A. S. Roy, S. P. Mudanai, D. Basu, and M. A. Stettler, "Compact model for ultrathin low electron effective mass double gate MOSFET," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 308–313, Feb. 2014, doi: 10.1109/TEDE.2013.2290779.
- [14] H. Wang, T.-L. Chen, and G. Gildenblat, "Quasi-static and nonquasi-static compact MOSFET models based on symmetric linearization of the bulk and inversion charges," *IEEE Trans. Electron Devices*, vol. 50, no. 11, pp. 2262–2272, Nov. 2003.
- [15] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. Hoboken, NJ, USA: Wiley, 2006, doi: 10.1002/0470855460.
- [16] *Users' Manual of Silvaco ATLAS, Version 5.20.2.R*. Accessed: May 2015. [Online]. Available: www.silvaco.com
- [17] G. Baccarani, E. Gnani, A. Gnudi, S. Reggiani, and M. Rudan, "Theoretical foundations of the quantum drift-diffusion and density-gradient models," *Solid-State Electron.*, vol. 52, no. 4, pp. 526–532, 2008, doi: 10.1016/j.sse.2007.10.051.
- [18] Y. S. Chauhan *et al.*, *FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard*. San Diego, CA, USA: Academic, 2015.

- [19] K. P. Ghatak, S. Bhattacharya, and D. De, *Einstein Relation in Compound Semiconductors and Their Nanostructures* (Springer Series in Material Science). Berlin, Germany: Springer, 2009.
- [20] Y. Tsvividis and C. McAndrew, *Operation and Modeling of the MOS Transistor* (The Oxford Series in Electrical and Computer Engineering). Oxford, U.K.: Oxford Univ. Press, 2011.
- [21] S. Jandhyala, R. Kashyap, C. Anghel, and S. Mahapatra, "A simple charge model for symmetric double-gate MOSFETs adapted to gate-oxide-thickness asymmetry," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1002–1007, Apr. 2012, doi: [10.1109/TED.2012.2184543](https://doi.org/10.1109/TED.2012.2184543).
- [22] N. Sharan and S. Mahapatra, "Nonquasi-static charge model for common double-gate MOSFETs adapted to gate oxide thickness asymmetry," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2419–2422, Jul. 2013, doi: [10.1109/TED.2013.2262943](https://doi.org/10.1109/TED.2013.2262943).
- [23] S.-Y. Oh, D. E. Ward, and R. W. Dutton, "Transient analysis of MOS transistors," *IEEE Trans. Electron Devices*, vol. ED-27, no. 8, pp. 1571–1578, Aug. 1980.
- [24] R. Venugopal, Z. Ren, S. Datta, and M. S. Lundstrom, "Simulating quantum transport in nanoscale transistors: Real versus mode-space approaches," *J. Appl. Phys.*, vol. 92, no. 7, p. 3730, 2002, doi: [10.1063/1.1503165](https://doi.org/10.1063/1.1503165).
- [25] C. Kittel, *Introduction to Solid State Physics*. Hoboken, NJ, USA: Wiley, 2005.



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